WHAT IS CLAIMED IS:

1. ~~A method of performing a conditional~~ vector ~~output operation in a processor, the method comprising~~:

receiving electrical signals representative of an input data vector;

generating electrical signals representative of a condition vector, the number of values in the input data vector being equal to the number of values in the condition vector, values in the input data vector and in the condition vector being in one-to-one correspondence with one another, and each value in the condition vector being a result of evaluating a predetermined conditional expression using data corresponding to a value in the input data vector; and

generating electrical signals representative of an output vector containing values in the input data vector for which corresponding values in the condition vector are equal to a predetermined value.

2. The method of claim 1, wherein the predetermined conditional expression is a Boolean expression.

3. The method of claim 1, further comprising generating electrical signals representative of at least one additional output vector containing values in the input data vector for which corresponding values in the condition vector are equal to a value corresponding to the output vector, the output vector and the at least one additional ~~output vector comprising a plurality of output vectors.~~

~~8. The method of claim 7 wherein calculating the partial indices includes performing a parallel prefix scan+ operation.~~

9. The method of claim 1 further comprising, after including the values within the group in the output vector, incrementing the running index by an amount corresponding to the number of values added to the output vector.

10. The method of claim 9 wherein the running index is incremented using a modular arithmetic operation.

11. The method of claim 10, wherein the modulus of the modular arithmetic operation is double the number of values added to the output vector.

12. The method of claim 1, wherein the running index and the absolute indices point to locations in at least one programmable memory.

13. The method of claim 12, wherein the absolute indices each include a first portion indicating one of a plurality of programmable memories and a second portion indicating an absolute location within that memory.

14. ~~The method of claim 1, wherein generating the plurality of output~~ vectors includes:

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4. The method of claim 3, wherein each element in the input data vector is in one and only one of the plurality of output vectors.

5. The method of claim 3, wherein generating the plurality of output vectors includes, for each value in the condition vector, including a corresponding value in the input data vector in one of the plurality of output vectors.

6. The method of claim 3, further comprising processing portions of the signals corresponding to each of the plurality of output vectors using the processor, the processing for at least two of the output vectors being different from one another.

7. The method of claim 1, wherein generating the output vector includes:

maintaining a running index indicative of a last-added value in the output vector;

for each value in a group of values from the input data vector corresponding to condition vector values which are equal to the predetermined value, calculating an absolute index indicative of a position of the value within an output vector value corresponding to the condition vector value and the running index; and

including each of the values within the group in an output vector corresponding to the condition vector values at respective positions denoted by the absolute indices.

storing values from the input data vector corresponding to values in the condition vector which are equal to one another in an intermediate memory; and

when the number of values thus stored equals a predetermined number, adding the values to one of the output vectors.

15. A method of performing a conditional vector input operation in a processor, the method comprising:

generating a plurality of electrical signals as condition data representative of whether individual arithmetic clusters in a plurality of arithmetic clusters are to receive data;

providing a plurality of electrical signals as input data to at least one arithmetic cluster in the plurality of arithmetic clusters for which a corresponding portion of the condition data is equal to a predetermined value;

using the arithmetic clusters to process the input data provided thereto; and

assembling the processed data to form an output vector.

16. A method according to claim 15 wherein a certain plurality of arithmetic clusters receive input data as a result of corresponding conditional data for said certain plurality of arithmetic clusters being said predetermined value.

17. A processor comprising:

a first memory element storing an input data value;

a second memory element storing a condition value;

a buffer element for storing an output data value;

a logic circuit which transfers the input data value from the first memory element to the buffer element when the condition value stored in the second memory element is equal to a predetermined value.

18. A processor comprising:

a first memory storing a plurality of input data values;

a second memory storing a plurality of condition values;

a buffer for storing a plurality of output data values;

a logic circuit which transfers an input data value from the first memory to the buffer when a corresponding condition value stored in the second memory is equal to a predetermined value.